

Why Do Authors and Seminar Leaders Disagree?

Douglas Brooks Ultracad Design, Inc

Introduction:

One of the more confusing things students and inexperienced designers run into is disagreements among authors or seminar leaders regarding why certain design guidelines should or should not be followed. I often got those types of questions in seminars (I am mostly retired now), and I just recently got another one (unedited except for omissions) by email:

I'm a young pcb designer started my career when i'm 18 three years ago. I had been through many design guidelines and used to refer many books including Douglas Brook's. I saw many test results and explanation of ... which contradicts with the design guidelines given by Douglas Brooks. When two great personalities of our industry have different opinions, it is us the poor designers who suffers to prove our self. I referred the book ... recently, those articles about differential pairs and its return path, having split planes etc really contradicts. (He) also proves with the test results that differential pair uses ground reference as return path and so can be routed in entirely different path and many more. It would be grateful if u give some justification.

Some Reasons for Disagreement:

There are several legitimate reasons for disagreement, and some lesser legitimate ones. (*In the following I am going to use the word "author" to refer generally to book and article authors, web site designers, and seminar leaders.*) For example:

Context A: Often an author Has a particular context in mind when he is talking about something. For example, he may be talking only about trace impedance control or EMI. Thus, the guidelines he is using may be correct for the context in which he is talking, but not in some other context, for example crosstalk.

There is a particularly interesting example in one of the most highly respected books. The author says he likes to rout differential pairs far apart to reduce differential coupling to zero. But the *context* of that discussion has nothing to do with signal integrity and everything to do with fabrication limits. Earlier he has said that (a) he was already using the narrowest traces his fabricator could handle, (b) he wanted to maintain 50 Ohm traces everywhere,

and (c) he wanted to maintain 100 Ohm differential impedance (without changing trace width.) Under those constraints he **MUST** eliminate coupling between the traces and therefore must route them far apart. If his constraints had been different, his conclusions might have been different.

Context B: Another author argues that routing traces across a split in the plane has no effect on trace impedance, and he even can reference studies that show that. But the problem is that there at least four reasons not to route a trace across a split in the plane — (1) impedance control, (2) EMI, (3) crosstalk control, (4) introduction of noise onto an unrelated plane. The author may be correct in the narrow context in which he is talking, but incorrect in the bigger picture.

Improper Generalization: I get particularly annoyed with authors who reject theory and insist on seeing data. Then they devise a study that "proves" a design rule does not need to be followed. This may or may not, in fact, be supported by that study (see below.) They then generalize from that result that the design rule **NEVER** has to be followed! I believe this is the worst disservice an author can provide to his/her readers.

Error: Some authors are just flat out wrong. I know of one so-called study in which the author routes a trace over a split in a plane, shows that there is no impact on impedance, and then generalizes from that that is always OK to route over a split. There are numerous things wrong with that conclusion. One of which is, of course, that trace impedance control is not the only reason for avoiding splits in planes. But in this particular study the author neglects to advise his readers about what is under the split plane (you only learn this if you look closely at the methodology.) Underneath the split is *another closely-spaced, related, unsplit plane!* This second plane completely nullifies the so-called result!

Conflicts: Some design rules are mutually exclusive! For example, I believe differential traces should be routed closely together (for EMI reasons) and should be the same length (for mode shift reasons.) Often these two design criteria

can't be met at the same time. (I believe the equal length one is the more important one.)

Honest Disagreement: There are some issues for which there is not uniform agreement among authors. For example, I personally believe that differential traces should be routed closely adjacent to each other. Other authors (many of whom I highly respect) disagree with me and I have had some spirited discussions with them. Their arguments (in this specific case) tend to focus on the idea that the return signal is underneath the trace, and therefore trace spacing is not the important issue. I believe that (a) it is not necessarily true that the return current is *always* under the trace. It is there only during the signal transition period (rise and fall time) but not necessarily during the stabilization time. During the stabilization time the signal is traveling the loop defined by the traces while the return loop on the board decays. In very high-speed logic, this may still create a possible EMI issue. And (b) even so, if separated traces pick up radiated noise, the further apart those traces are the greater will be the common mode component of that noise.

As an aside, most of us agree that the *primary* design constraint with differential traces is that they should be the same length to avoid mode shift during signal travel. Also most of us agree that if there are no signal integrity issues with a particular design, then there are no necessary differential trace design rules either!

All I can say regarding issues like this is what we, at UltraCAD, believe. And we have a very good track record with our design results.

Resource Limitations:

I once had a student observe that computer motherboards and memory modules seemed to break almost every design rule we discussed in class. A friend who is active on the seminar circuit designs the motherboards for one of the major microprocessor manufacturers. I asked him one time how many iterations he went through in optimizing the design for their latest (at the time) motherboard. His answer was:

"13, but the first design did boot up!"

Most of us don't have the resources to design, build, and test 13 iterations of a design in order to optimize it. (And to tell the chip designer to change the pinout locations of the microprocessor package!) Most of us get one or two shots at the design. Therefore, we have to approach the design more conservatively, using design rules that are known to be effective, even if perhaps they turn out to be overkill in a specific situation.

Final Thoughts:

Signal integrity issues are very situation- and design-specific. A technique that works in one situation may not work in another. A design practice that may cause EMI in one instance has that EMI shielded and/or neutralized in another instance. Ground bounce or crosstalk that can interfere with system logic in one instance may not do so in a different circuit with different timing or noise margin conditions.

A fully trained and experienced senior engineer may (but may not) know when design issues may or may not impact his or her design. But most board designers do not have that level of training or experience. Therefore, most of us have to approach the design more conservatively.

But here is the bottom line. Designers, when you attend seminars and read articles, don't just memorize the design rules. Read to understand *WHY* the author is recommending certain rules, and what the *CONTEXT* of the discussion is. Don't react to a design rule that says don't route a trace across a plane split. Try to understand *WHY* you should not route across a plane split and what things might happen if you do. If design rules conflict (and they sometimes do) you can only make an informed judgment as to which one to choose if you understand the reasons behind the rules.

Finally, it often happens that we must compromise some rules in order to meet other design constraints. This is not bad, per se. It happens to all of us. But when you do so, be aware that such a compromise *might* impact performance. And you can only have this awareness if you *understand* the reasoning behind the various rules in the first place. Then if the design does happen to fail in some way, you will know some places to look first for a solution to the problem.

ABOUT THE AUTHOR:



Douglas Brooks is president of UltraCAD Design, Inc., a PCB design service bureau in Bellevue, WA, that specializes in large, complex, high density, high speed designs. He has been a frequent contributor to various magazines and has given PCB Design seminars around the world. He can be reached at dgbarticles@dgbpersonal.com.