POWER DISTRIBUTION SYSTEM

Calculating PDS Impedance

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On a PCB (Printed Circuit Board) the Power Distribution System (PDS) is the system that distributes power from the power source to the various chips and devices requiring power. This system can range from being very simple to being very complex.

A simple system may receive its power from some source off the board, probably through an edge connector. It then distributes the power to the devices by traces routed from the edge connector to the devices.

A complex system may involve one or more regulated power supply circuits on the board. The power may be "conditioned" by filters as simple as a bulk capacitor to as complex as sophisticated multistage LC filter circuits. The power is then distributed around the board on a system of planes, probably including at least one set of closely spaced Power/Gnd planar pairs for distributed planar capacitance. (Side note: Strictly speaking, it is incorrect to call the return plane a "ground" plane. As Bruce Archambeault (Note 1) is fond of saying, "Ground is a place where potatoes and carrots grow!" The return plane is more properly called the "reference" plane. Every power plane should have an associated reference plane. I often use the term "ground plane" out of habit and for historical reasons.)

The PDS has three primary requirements it must satisfy. It must:

1. Deliver a well-regulated voltage that is
2. Stable at all points on the board under all current (loading) conditions, and is
3. Quiet.

These requirements are typically achieved as follows:

1. Power regulation is achieved at the regulated power supply circuit, supported by one or more bulk capacitors and (LC) filtering circuits. (Some of these filtering circuits are available as monolithic chips.) A typical bulk filtering capacitor will have a value of at least several microfarads, often much more.

2. Stability under all loading conditions actually has two dimensions:

(a) The first requirement is that the distribution system have low resistance and inductance. This usually requires a system of power/return planes for distribution and low inductance pads/vias at the various device connections.

(b) The second requirement is that the charge (current is the flow of charge per unit time; see Brooks, Note 2) be available where and when needed. This is a subtle requirement that is not clearly understood by some people. Charge (current) flows at the rate of (approximately) 6"/ns on a board fabricated with FR4. If a device switches a significant amount of current (i.e. a significant amount of charge) in 1.0 ns, that charge must be within 6" of the requirement. Half of the charge must be with 3" of the requirement. One quarter of the charge must be within 1.5" of the requirement. A large board with a regulated power supply more than 6" away cannot supply the charge required by the switching device fast enough. The required charge is typically stored in bypass capacitors that we routinely place around the board (some of which are fortuitously close enough to meet the various requirements), and to a lesser extent from distributed planar capacitance.

3. "Quiet" means that when a device switches it does not generate "noise" on the board that interferes with other devices or generates EMI. The fundamental source of switching noise is inductance and the relationship V = L * di/dt (noise voltage is inductance multiplied by the switching current divided by the switching rise time.) Even with very low inductance circuits, switching circuits with very fast rise times (very small dt) can generate destructive levels of noise. "Quiet" PDSs are achieved with very close attention to low inductance paths, low inductance pads and vias, and planar capacitance. (See Hartley, note 3)

Traditionally, we have understood that a good, quiet PDS is one that had a lot of bypass capacitors on it. And it was easy to extend this understanding to the concept that more (bypass capacitors) is better. But there is another, better way to look at this whole issue. Consider that the power distribution system has lots of bypass capacitors between the power and reference

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planes. That means that the AC impedance between the power and reference planes is quite low (in simplistic terms, the power and reference planes are "shorted out" at higher frequencies by the bypass capacitors.) Let's change our thinking about the PDS as follows:

The IDEAL Power Distribution System has infinite impedance at DC (for DC power distribution) and zero impedance at all other frequencies (no matter how we achieve this.)

The ideal is, of course, not possible to achieve. But you get the point. What we need is high impedance at DC, and very low impedance everywhere else, see Figure 1. Then power gets distributed where we need it and the system is inherently quiet. And we did not say we needed bypass capacitors to achieve this ideal, although if we throw enough bypass capacitors at the system we will approximate it (at least theoretically).

Let's look at some possible PDS configurations. Figure 2 shows an impedance curve for a system with 50 each .01 uF capacitors. In the real world, capacitors (and their mounting) have some inductance associated with them, so let's assume for this illustration that the associated inductance with each one is 5.0 nH. And, capacitors have some ESR associated with them, so let's also assume that the ESR for each capacitor is 0.01 Ohms. Those are the assumptions behind the curve in Figure 2. As a matter of reference, a horizontal line is drawn on the curve at 0.1 Ohms impedance.

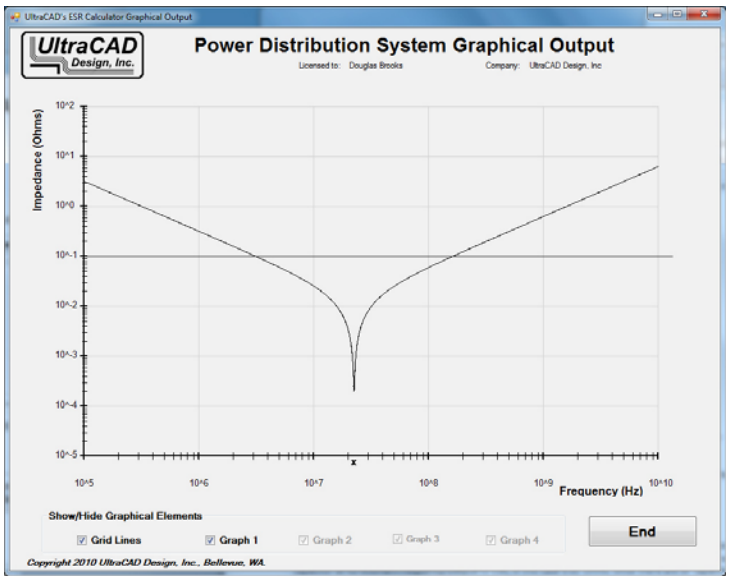

Figure 2
50 each .01 uF capacitors. The horizontal line is a 0.1 Ohms reference.

The negative spike in the impedance curve occurs at the self-resonant frequency of the capacitors. That frequency is given by:

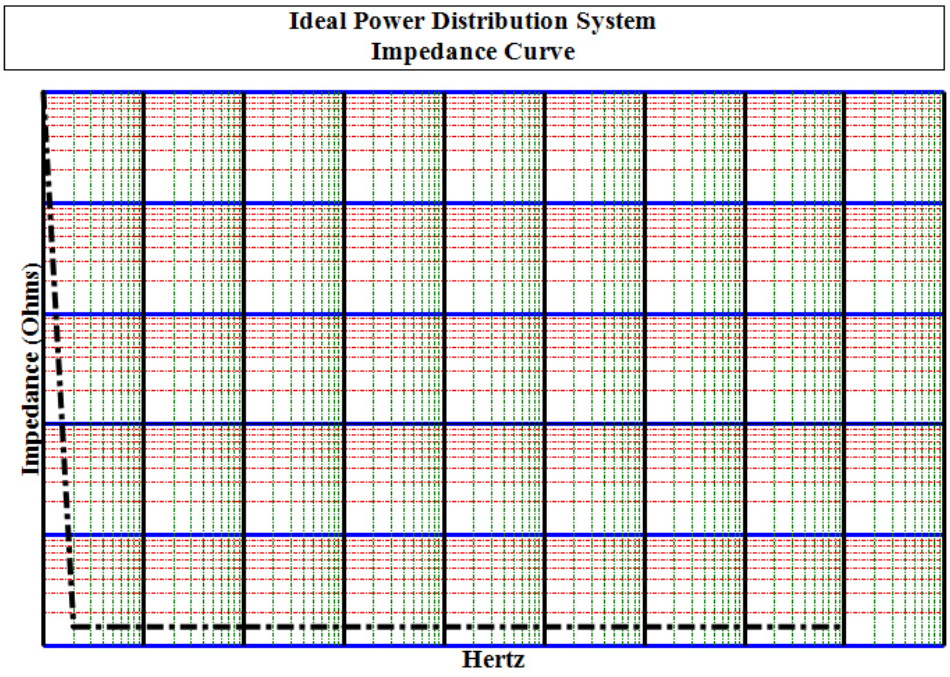

Figure 1.
The ideal power distribution system impedance curve would be very high at DC and low at

$$f_r = \frac{1}{2*\pi*\sqrt{L*C}} = 22.5 \text{ MHz} \qquad \text{Equation 1}$$

where C = 0.01 uF and L = 5.0 nH. Each capacitor, along with its associated inductance, forms a series LC circuit. LC circuits have a self-resonant frequency as specified in Equation 1. The impedance of each such capacitor at its resonant frequency is equal to ESR, in this case 0.01 Ohms. Since there are 50 capacitors in parallel in this design, the net impedance at the self-resonant point is 0.01/50 = 0.0002 Ohms, as shown in Figure 2.

This design does not meet our requirements (high impedance at DC, low impedance everywhere else), but we can at least see a tendency. Suppose we modify the design to include some .001 uF capacitors. Specifically, suppose we add 50 each .001 capacitors, with associated inductance equal to 5.0 nH each and each with an ESR of .01 Ohms to the 50 each .01 capacitors we already have. Figure 3 is the resulting PDS Impedance Curve from those assumptions.

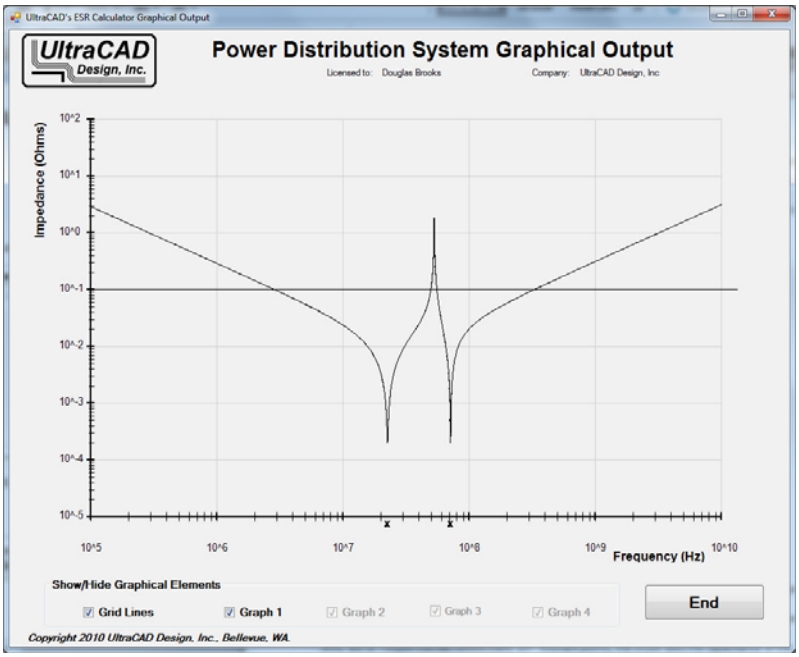

Figure 3.
50 each .01 and 50 each .001 capacitors.

The results are better; except for that disturbing impedance peak at approximately 52.8 MHz. That peak is known as an "anti-resonant" peak (really a parallel resonant peak) between the self-resonant frequencies of the two capacitor values we are using. Under our assumptions, the .01 capacitors have a self-resonant frequency at 22.5 MHz and the .001 capacitors have a self resonant frequency at 71.2 MHz. But at frequencies BETWEEN these self-resonant points, the circuit sees the capacitance of the .001 capacitor in parallel with the inductance of the .01 capacitor. This results in a parallel (or anti-) resonance at a frequency in between, in this case about 52.8 MHz. The problem in this case is that the PDS as designed here is pretty quiet out to around 400 MHz, except in the region around 52 to 53 MHz. This is BAD. The practical consequences of this is that if there are any noise frequencies on our board in this frequency region (say caused by a clock or data frequency harmonic) those frequencies will not be attenuated by PDS and may ultimately become radiated EMI. When boards fail to pass FCC compliance testing, it is not unusual to find that the frequencies where they fail are in the region of PDS anti-resonant points.

At this point it should be clear where we are going. Two very relevant questions are:

1. Can I design a PDS system so there are no anti-resonant points, or at least where the impedance at all frequencies within a range is below some target impedance? And

2. How can I calculate the impedance of my PDS?

The answer to ther first question is "Yes!"(See Brooks, note 4.) As Brooks showed in that article, *in very general terms*:

1. More capacitors are better than fewer capacitors.
2. More capacitor ***values*** are better than fewer capacitor ***values***.
3. Moderate ESR is better than lower ESR.

But the answer to the second question is much more problematic. Think in these terms. A single bypass capacitor is really a series RLC circuit (its inherent capacitance, its inherent inductance along with the inductance of the mounting and bonding system, and its ESR.) Manually calculating an impedance curve for a single RLC circuit is straightforward. If we have two such capacitors

in parallel, manually calculating the resulting impedance curve is manageable, but more difficult. Manually calculating the impedance curve for three such capacitors in parallel is a pretty good challenge. Manually calculating the impedance curve of hundreds of capacitors in parallel in unthinkable.

There are tools that can by used for such analyses, but they are often not designed for practical sets of calculations. The last time I used Excel for such an analysis it simply boged down under the shear amount of data it was processing.

So we at UltraCAD created our own calculator for calculating the impedance of a power distribution system. See it at http://www.ultracad.com/calc.htm. The primary form for the calculator is shown in Figure4.

The calculator can be used in two modes, (a) Use internally defined values, and (b) Input values from file. The first is useful for experimenting with various options --- number of capacitor values, values for capacitance and inductance, impact of ESR, etc. --- and seeing what the impact is on overall impedance. Figures 2 and 3 were generated using this function. The second allows the user to enter data that represents his/her actual PDS. The calculator will then generate in impedance curve that represents that data.

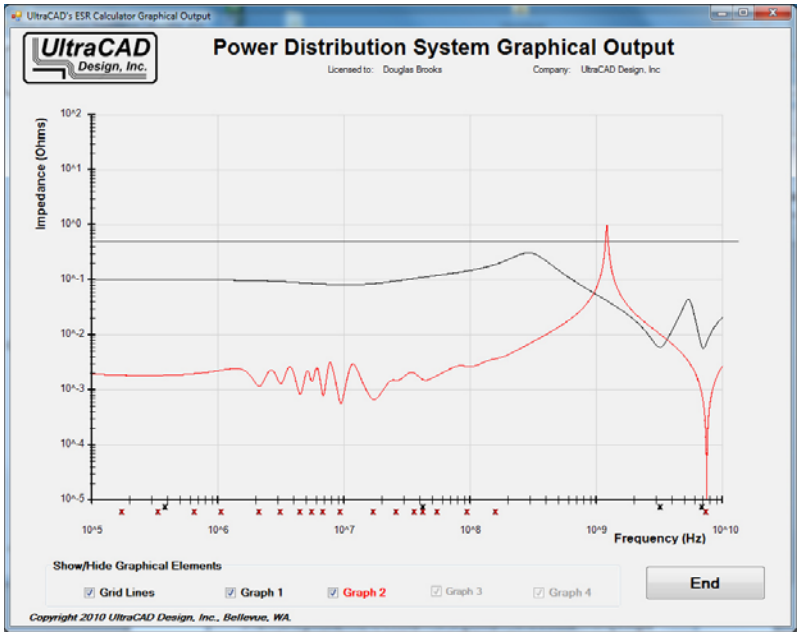

Figure 5.
Results from two different users' data files.

Two licensed users of an earlier version of this calculator were nice enough to send us copies of their data files. They have given us permission to use the files, but not to identify them or their companies. Figure 5 shows the results from these two data files. An arbitrary reference line is drawn at 0.5 Ohms on the output. Test sample 1 is safely below that value at all points, Test sample 2 has an antiresonance that just exceeds this value in one small area. Both of these illustrations employ one or more planar capacitance pairs in their design. People who purchase a license for this calculator get copies of these two test files in their package.

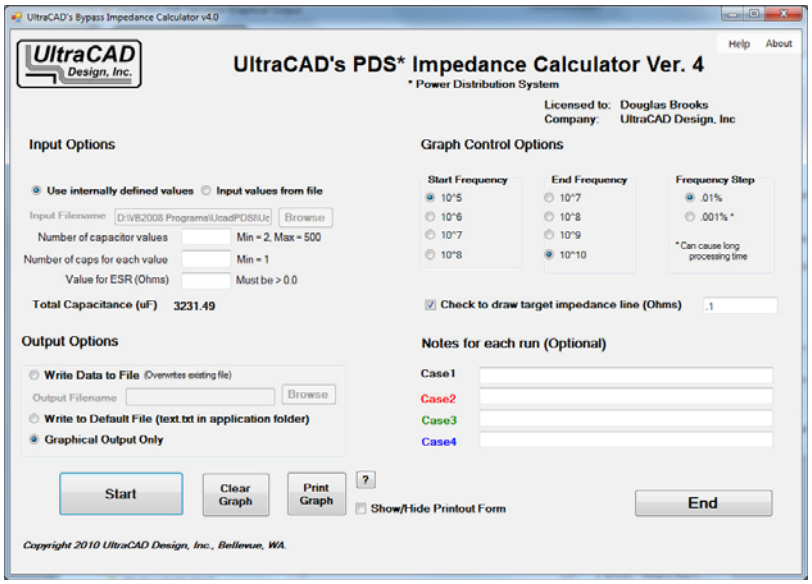

Figure 4.
UltraCAD's Power Distribution System Impedance Calculator.

Summary:

Looking at the power distribution system impedance curve of a PCB can by quite useful in designing or troubleshooting circuit boards. Knowing where the anti-resonant point are can be especially useful. The concept of an "ideal" PDS impedance curve can be very useful picture to keep in mind.

References:

1. Bruce Archambeault is fond of saying this in his articles and seminars. See also his PCB Design for Real-World EMI Control, Springer publications, July, 2002.

2. Brooks, "What is This Thing Called 'Current:' Electrons, Displacement, Light, or What?" available at http://www.ultracad.com/mentor/what_is_current.pdf

3. Rick Hartley, *Controlling Radiated EMI Through PCB Stack-Up*, "Printed Circuit Design", July, 2000, p16. Although Rick's article was narrowly pointed at radiated EMI, his conclusions are quite general. The two primary guidelines for good signal integrity performance are (a) route every trace close to a continuous, related reference plane, and (b) use at least one power/ground planar pair for planar capacitance.

4. See Brooks, "ESR and Bypass Capacitor Self Resonant Behavior: How to Select Bypass Caps," available at http://www.ultracad.com . You can see the PDSI calculator at http://www.ultracad.com/calc.htm . An Operator's Manual/Help file can be downloaded from there to learn more about the calculator, its capabilities, and how to program it.

ABOUT THE AUTHOR:

Douglas Brooks has his MS/EE from Stanford University and a PhD from the University of Washington. He has spent most of his career in the electronics industry in positions of engineering, marketing, general management, and as CEO of several companies. He has owned UltraCAD Design, Inc. since 1992. He is the author of numerous articles in several disciplines, and has written articles and given seminars all over the world on Signal Integrity issues since founding UltraCAD. His book, Printed Circuit Board Design and Signal Integrity Issues was published by Prentice Hall in 2003. His web page can be found at http://www.ultracad.com .